SILICON BASED MOS STRUCTURES WITH A TiO_2 LAYER GROWN BY ATOMIC LAYER DEPOSITION FOR SOLAR FUEL GENERATION

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1. Introduction

The current developments in the field of solar fuel generation require, in addition to mastering the growth of nano-sized thin metal oxide layers with insulating properties, also understanding the complex processes of the photovoltaic generation of charge carriers, their flow kinetics and the electrochemical effect of their flow upon water decomposition. In this respect, good prospects belong to metal-insulator-semiconductor (MIS) structures in which the insulating layer predominantly consists of a thin layer of metal oxides. The properties of such MOS structures differ from the widely used unipolar electronic devices, namely by special requirements for the conductivity and stability of the thin oxide layers [1, 2].

A photoelectrochemical water decomposition device typically employs a top thin metallic film catalysing the water oxidation reaction. The top metallic film has to be transparent for sun light, must exhibit catalytic activity, corrosion resistance, high work function and low resistivity [3]. It was shown that operation of a Si-based photoanode during long-duration of oxygen evolution can be significantly improved by covering the anode by a thin TiO_2 layer [4, 5].

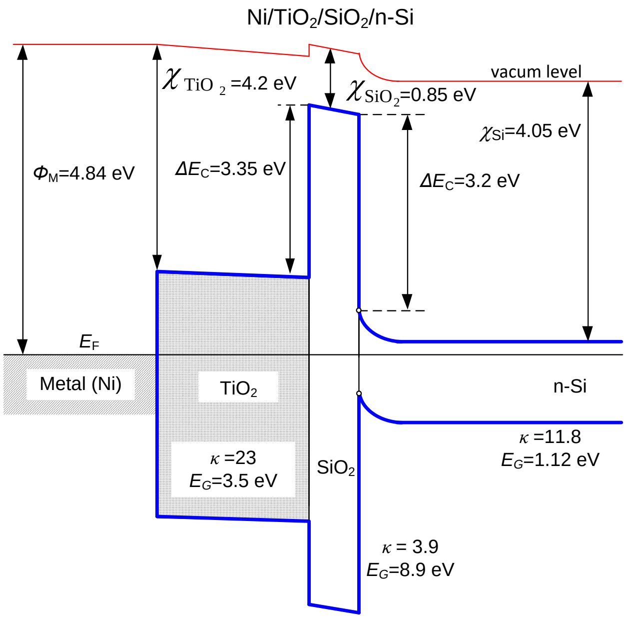
2. Experiment

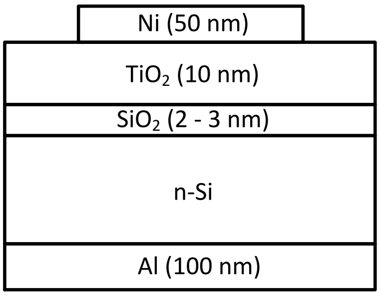
In our contribution we have examined the properties of Si photoanodes covered by TiO_2 and Ni thin films.

The MOS structures were prepared by atomic layer deposition (ALD) of a 10.3 nm thin TiO_2 layer on an n-type silicon substrate (n-Si) with a native SiO_2 layer. The silicon wafer with orientation (100), thickness of 625 μm and resistance of 5 to 8 Ωcm was used as a substrate. The thin film of native SiO_2 oxide (2 to 3 nm) was not removed prior to deposition of the TiO_2 layer. The TiO_2 film was grown by thermal ALD at 150 °C using titanium isopropoxide and water as precursor and reactant, respectively. Three annealing conditions were used for post-deposition processing of TiO_2/SiO_2/n-Si structures in forming gas
(95% N_2 + 5% H_2) for 60 minutes: different temperatures 400 °C, 500 °C and 600 °C. After annealing, the top emitter contact was prepared by evaporation of a 50 nm thick nickel layer with various photolithographically patterned areas of the gates.

The bottom contact was created by evaporating a full area aluminium contact onto the back side of silicon. Figure 1 shows the band diagram, cross-sectional view of the structure and sample labelling referring to the temperature of annealing.

Current-voltage (*I*-*V*) measurements were carried out in dark and under light of a halogen lamp using Keithley 2612.





Samples	Annealing
FG 0	reference
FG 400	400°C
FG 500	500°C
FG 600	600°C

Fig. 1: Band diagram of the Ni/TiO_2/SiO_2/n-Si structure, cross-sectional view of the structure and sample labelling.

3. Results and discussion

Figure 2 shows typical *I-V* curves of samples annealed at different temperatures as compared with a non-annealed reference sample. On the *I-V* curve of the forward biased non-annealed reference sample FG0 one can see a small kink. As the annealing temperature increases, the height of this kink increases to about 400 °C. With a further increase in annealing temperature, this shape on the *I-V* curves gradually vanishes. At annealing temperatures above 500 °C, the kink disappears completely. It turns out that the size of the kink is directly related to the photovoltaic response of the structure. This relationship results from the comparison of dark (Fig. 2) and light (Fig. 3) *I-V* curves. It is obvious that the larger the kink in the dark curve, the stronger the photovoltaic response of the Ni/TiO_2/SiO_2/n-Si structure under light. To explain this phenomenon it is necessary to understand the current mechanism responsible for this anomaly in the *I-V* curve.

The transfer of the charge through the insulating oxide layer is mediated by tunnelling of free charge carriers between the metal (Ni) and the semiconductor (n-Si). First, direct tunnelling of electrons between the metal and the conduction band of the semiconductor is considered. The intensity of direct tunnelling depends on the height of the potential barrier formed by the insulating layer and on the effective tunnelling mass of the electrons. It is therefore believed that this current mechanism will not be affected by the annealing technology. In addition, theoretical simulations on a similar structure published in [6] have shown that the contribution of direct tunnelling to the total current is almost negligible.

Therefore, it remains to look for the cause of the kink anomaly in trap-assisted-tunnelling (TAT). In this type of indirect tunnelling, the interface between the insulator and the semiconductor plays a crucial role. With this current conduction mechanism, the electrons of the metal tunnel into the traps on the interface and by thermionic emission they enter the conduction band of the semiconductor, and reversely, by recombination the electrons from the conduction band are captured by unoccupied interface traps from where they tunnel back to the metal. Obviously, the magnitude of these currents depends on the density of traps (most likely oxygen vacancies) at the interface, more precisely on the energy distribution of the trap density in the forbidden band of the semiconductor. This trap density distribution is influenced by the sample preparation technology and by the annealing temperature.

Simulations reveal that the trap density distribution has Gaussian distributions with one maximum between the centre of the energy gap and the conduction band of the semiconductor, and another one between the middle of the forbidden band and the valence band. The existence of these Gaussian peaks gives rise to the typical current kink. The greater the density of traps in the top Gaussian maximum, the more pronounced the jump in the dark *I-V* curve. At high annealing temperatures, above 400 °C, the density of defects, mainly of oxygen vacancies, increases, forming the bottom Gaussian peak.

The photovoltaic response and the quality of the structure were measured by light *I-V* measurements (Fig. 3). The photovoltaic phenomenon in Ni/TiO_2/SiO_2/n-Si structures requires suitable conditions for the transport of light-generated charge carriers through the thin oxide layer and suppression of the recombination of minority holes at the interface between the silicon and the oxide layer. Under light, photons interact with electrons trapped in the surface danglig bond states. This provides them with additional energy needed for emission to the conduction band hereby increasing the TAT flow rate in a reverse biased Ni/TiO_2/SiO_2/n-Si structure as shown in Fig. 3, curves FG0 and FG400. Comparing such samples, only FG400 exhibits a photovoltaic response with an open circuit voltage V_{OC}≈0.45 V and short circuit current J_{SC}≈20 μA.

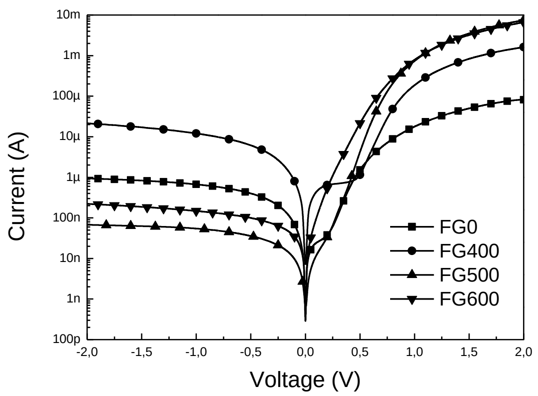


Fig. 2: Dark *I-V* curves of samples annealed in the forming gas.

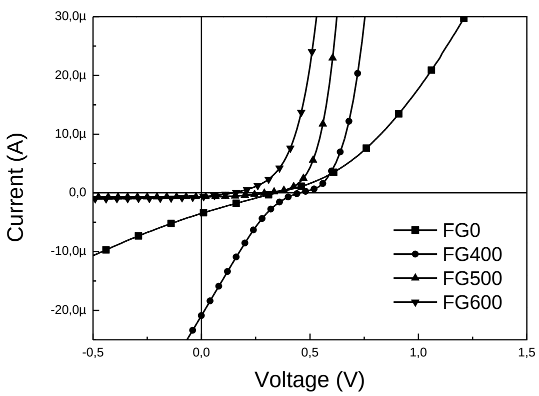


Fig. 3: Light *I-V* curves of samples annealed in the forming gas.

4. Conclusion

The paper presents the results of electrical measurements of MOS photoanodes with SiO_2 and TiO_2 dielectric layers annealed at different temperatures in the forming gas. Annealing at 400 °C leads to the highest photovoltaic response, which was due to both the low defect state density at the interface and indirect tunnelling of photo-generated holes via insulator-to-semiconductor interface traps. Annealing in the forming gas at a temperature above 400 °C brings about a low interface quality resulting in a negligible photovoltaic response. Based on this study, the post-deposition annealing in at 400 °C results in the best photo-electrochemical response.

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